AF/2819/#

PTO/SB/17 (10-03)
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☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) 330.00

Complete if Known	
Application Number	10/052,652
Filing Date	January 18, 2002
First Named Inventor	Ronalf Kramer
Examiner Name	Tan, Vibol
Art Unit	2819
Attorney Docket No.	1406/36

METHOD OF PAYMENT *(check all that apply)*

☐ Check ☐ Credit card ☐ Money Order ☐ Other ☐ None

☒ Deposit Account:

Deposit Account Number: 50-0426

Deposit Account Name: Jenkins, Wilson & Taylor, P.A.

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FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1001	770	2001	385	Utility filing fee	
1002	340	2002	170	Design filing fee	
1003	530	2003	265	Plant filing fee	
1004	770	2004	385	Reissue filing fee	
1005	160	2005	80	Provisional filing fee	

SUBTOTAL (1) ($) 0.00

2. EXTRA CLAIM FEES FOR UTILITY AND REISSUE

	Extra Claims		Fee from below		Fee Paid
Total Claims		-20** =		X	=
Independent Claims		- 3** =		X	=
Multiple Dependent					=

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
1202	18	2202	9	Claims in excess of 20
1201	86	2201	43	Independent claims in excess of 3
1203	290	2203	145	Multiple dependent claim, if not paid
1204	86	2204	43	** Reissue independent claims over original patent
1205	18	2205	9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($) 0.00

**or number previously paid, if greater; For Reissues, see above

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1051	130	2051	65	Surcharge - late filing fee or oath	
1052	50	2052	25	Surcharge - late provisional filing fee or cover sheet	
1053	130	1053	130	Non-English specification	
1812	2,520	1812	2,520	For filing a request for *ex parte* reexamination	
1804	920*	1804	920*	Requesting publication of SIR prior to Examiner action	
1805	1,840*	1805	1,840*	Requesting publication of SIR after Examiner action	
1251	110	2251	55	Extension for reply within first month	
1252	420	2252	210	Extension for reply within second month	
1253	950	2253	475	Extension for reply within third month	
1254	1,480	2254	740	Extension for reply within fourth month	
1255	2,010	2255	1,005	Extension for reply within fifth month	
1401	330	2401	165	Notice of Appeal	
1402	330	2402	165	Filing brief in support of an appeal	330.00
1403	290	2403	145	Request for oral hearing	
1451	1,510	1451	1,510	Petition to institute a public use proceeding	
1452	110	2452	55	Petition to revive - unavoidable	
1453	1,330	2453	665	Petition to revive - unintentional	
1501	1,330	2501	665	Utility issue fee (or reissue)	
1502	480	2502	240	Design issue fee	
1503	640	2503	320	Plant issue fee	
1460	130	1460	130	Petitions to the Commissioner	
1807	50	1807	50	Processing fee under 37 CFR 1.17(q)	
1806	180	1806	180	Submission of Information Disclosure Stmt	
8021	40	8021	40	Recording each patent assignment per property (times number of properties)	
1809	770	2809	385	Filing a submission after final rejection (37 CFR 1.129(a))	
1810	770	2810	385	For each additional invention to be examined (37 CFR 1.129(b))	
1801	770	2801	385	Request for Continued Examination (RCE)	
1802	900	1802	900	Request for expedited examination of a design application	

Other fee (specify) _____

*Reduced by Basic Filing Fee Paid

SUBTOTAL (3) ($) 330.00

SUBMITTED BY				(Complete *(if applicable)*)	
Name *(Print/Type)*	Richard E. Jenkins	Registration No. *(Attorney/Agent)*	28,428	Telephone	001-919-493-8000
Signature	Richard E. Jenkins			Date	March 1, 2004

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This collection of information is required by 37 CFR 1.17 and 1.27. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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March 1, 2004

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on March 1, 2004.

Angela L. Boyd
Date of Signature March 1, 2004

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Re: U.S. Patent Application Serial No. 10/052,652 for
CIRCUIT FOR GENERATING AN ASYNCHRONOUS SIGNAL PULSE
Our File No. 1406/36

Sir:

Please find enclosed the following:

1. Fee Transmittal Form (PTO/SB/17 - 1 pg) in duplicate;

2. Three (3) duplicate originals of Appeal Brief (19 pgs each/ total of 57 pgs); and

3. A return-receipt postcard to be returned to our offices with the U.S. Patent and Trademark date stamp thereon.

Please contact our offices if there are any questions with respect to this matter.

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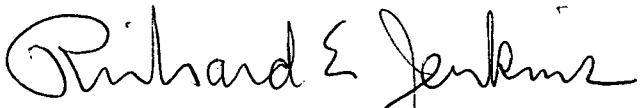
The Commissioner is hereby authorized to charge any fees associated with the filing of this correspondence to Deposit Account No. **50-0426**.

Respectfully submitted,

JENKINS, WILSON & TAYLOR, P.A.



Richard E. Jenkins
Registration No.: 28,428
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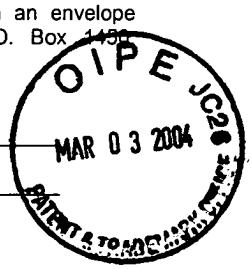
REJ/BJO/alb

Enclosures

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on March 1, 2004.

Angela L. Boyd
Date of Signature March 1, 2004



PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Kramer

Group Art Unit: 2819

Serial No.: 10/052,652

Examiner: Vibol Tan

Filed: January 18, 2002

Docket No.: 1406/36

Confirmation No.: 5317

For: CIRCUIT FOR GENERATING AN ASYNCHRONOUS SIGNAL PULSE

* *

APPEAL BRIEF

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

I. Real Party in Interest

Infineon Technologies AG is the real party in interest.

II. Related Appeals and Interferences

There are no other appeals or interferences, known to applicant, or applicant's legal representatives, which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

III. Status of Claims

Claims 1, 3–11, and 15–17 are pending in this application. Claims 1, 3–11, and 15–17 have been rejected. Claim 2 has been cancelled. Claims 12–14 were not entered. Claims 15–17 have been objected to because of informalities. The rejections of Claims 1, 3–11, and 15–17 under 35 U.S.C. §103(a) are appealed herein.

IV. Status of Amendments

Amendments A, B, and C were filed on February 5, 2003, June 16, 2003, and August 25, 2003, respectively. The Examiner issued a Final Rejection following Amendment A and an Advisory Action following Amendment B. Applicant filed a Request for Continued Examination (RCE) with Amendment C following the Advisory Action. The Examiner rejected the claims of Amendment C under 35 U.S.C. §103(a) in an Office Action dated September 22, 2003.

Applicant and the Examiner conducted a Telephone Interview on February 11, 2004 following the Office Action dated September 22, 2003. During the Telephone Interview, the Examiner indicated that he did not believe that the application contained patentable subject matter in view of the cited references. Furthermore, the Examiner indicated that an Appeal was applicant's only available option to obtain allowance of the application. Therefore, applicant and the Examiner agreed to an Appeal although the last Office Action was not a final rejection. A Notice of Appeal was filed on February 23, 2004.

V. Summary of Invention

The subject matter of the application is directed to a circuit for generating a single asynchronous signal pulse at an output of an integrated circuit. The signal pulse can be generated when a first and second control pulse is applied. For example, Claim 1 recites an integrated circuit **1** comprising a push-pull driving circuit having a first transistor **2** and second transistor **3** including control terminals **G1** and **G2**, respectively, being independently controlled by different control pulses (**A** and **B**) between a first and second supply potential ($\mathbf{U_{DD}}$ and **GND**, respectively). Application, page 3, line 30, to page 4, line 18; and Figures 1A and 1B. Claim 1 also recites a centre tap connected with an output terminal **4** of integrated circuit **1**. Application, page 4, lines 20-26; and Figures 1A and 1B. Further, Claim 1 recites a single resistor **6** or **7** being externally coupled with the output terminal of the integrated circuit and being of a pull-up or pull-down type. Application, page 5, lines 30-37; and Figures 1A and 1B. The type of resistor can determine, by application of a first control pulse on control terminal **G2** of the second transistor **3** and then a second control pulse on the control terminal **G1** of the first transistor **2**, whether a single positive or a single negative control pulse (**B** and **A**, respectively) is applied on output terminal **4**. Application, page 6, lines 1-15; and Figures 1A and 1B. Claim 1 also recites a waiting time **Δt** between first control pulse **B** and second control pulse **A** such that the two pulses do not overlap. Application, page 6, lines 26-31; and Figures 1A and 1B. Therefore, the application of an externally-coupled, pull-up or pull-down resistor (**6** or **7**, respectively) determines whether the single pulse is a

single negative or a single positive control pulse (**A** or **B**, respectively). Application, page 5, line 30, to page 6, line 8; and Figures 1A and 1B. This feature is advantageous because the negative or positive control pulse (**A** or **B**, respectively) is provided at the output without special settings, such as circuit programming. Claims 3–5, and 15 depend from Claim 1.

Independent Claim 6 recites a circuit **1** for generating a negative signal pulse in response to receiving a sequence of a positive and negative control pulse (**B** and **A**, respectively). Application, page 6, lines 1-8; and Figures 1A and 2. Claim 6 also recites a first transistor **2** including a control terminal **G1** and a load path connected between an output terminal **4** and a first supply potential $\mathbf{U_{DD}}$ for receiving a negative control pulse at control terminal **G1**. Application, page 4, lines 9-18; and Figure 1A. Further, Claim 6 recites a second transistor **3** including a control terminal **G2** and a load path connected between output terminal **4** and a second supply potential **GND** having a potential less than first supply potential $\mathbf{U_{DD}}$ for receiving a positive control pulse at control terminal **G2** in a sequence with control terminal **G1** of first transistor **2** receiving the negative control pulse. Application, page 4, lines 9-18; and Figure 1A. Claim 6 also recites a pull-up resistor **6** connected between first supply potential $\mathbf{U_{DD}}$ and output terminal **4** for generating a negative signal pulse at output terminal **4** in response to control terminals **G1** and **G2** receiving the sequence of negative and positive control pulses. Application, page 6, lines 1-8; and Figure 1A. Claims 7, 8, and 16 depend from Claim 6.

Independent Claim 9 recites a circuit **1** for generating a positive signal pulse in response to receiving a sequence of a positive and negative control pulse (**B** and **A**, respectively). Application, page 6, lines 10-15; and Figures 1B and 2. Claim 9 also recites a first transistor **2** including a control terminal **G1** and a load path connected between an output terminal **4** and a first supply potential $\mathbf{U_{DD}}$ for receiving a negative control pulse at control terminal **G1**. Application, page 4, lines 9-18; and Figure 1B. Further, Claim 9 recites a second transistor **3** including a control terminal **G2** and a load path connected between output terminal **4** and a second supply potential **GND** having a potential less than first supply potential $\mathbf{U_{DD}}$ for receiving a positive control pulse at control terminal **G2** in a sequence with control terminal **G1** of first transistor **G1** receiving the negative control pulse. Application, page 4, lines 9-18; and Figure 1B. Claim 9 also recites a pull-down resistor **7** connected between second supply potential **GND** and output terminal **4** for generating a positive signal pulse at output terminal **4** in response to control terminals **G1** and **G2** receiving the sequence of negative and positive control pulses. Application, page 6, lines 10-15; and Figure 1B. Claims 10, 11, and 17 depend from Claim 9.

VI. Issues

Whether the claims of applicant's invention are obvious under 35 U.S.C. §103(a) by the combined teachings of U.S. Patent No. 5,469,081 to Horita et al. (hereinafter, "Horita") and U.S. Patent No. 6,160,417 to Taguchi (hereinafter, "Taguchi").

VII. Grouping of Claims

It is believed that Claims 1, 3–11, and 15–17 do not stand or fall together.

Independent Claims 1, 6, and 9 stand or fall independent of each other as well as the claims dependent therefrom. Claim 1 recites an integrated circuit comprising a push-pull driving circuit having a first and second transistor including control terminals being independently controlled. Claim 6 recites a first and second transistor and a pull-up resistor for generating a negative signal pulse in response to receiving a sequence of negative and positive control pulses. Claim 9 recites a first and second transistor and a pull-down resistor for generating a positive signal pulse in response to receiving a sequence of negative and positive control pulses. It is believed that these features patentably distinguish Claims 1, 6, and 9, as each claim recites different structure. Applicant believes that these claims, subject to the same type of rejection, are separately patentable.

Claims 3–5, and 15 each stand if Claim 1 stands, but each claim adds a limitation to the circuit recited in Claim 1 which may enable these claims to stand separately even if Claim 1 falls.

Claims 7 and 8 each stand if Claim 6 stands, but each claim adds a limitation to the circuit recited in Claim 6 which may enable these claims to stand separately even if Claim 6 falls.

Claims 10 and 11 each stand if Claim 9 stands, but each claim adds a limitation to the circuit recited in Claim 9 which may enable these claims to stand separately even if Claim 9 falls.

Claim 15 stands if Claim 1 stands, but the claim adds a limitation to the circuit recited in Claim 1 which may enable the claim to stand separately even if Claim 1 falls.

Claim 16 stands if Claim 6 stands, but the claim adds a limitation to the circuit recited in Claim 6 which may enable the claim to stand separately even if Claim 6 falls.

Claim 17 stands if Claim 9 stands, but the claim adds a limitation to the circuit recited in Claim 9 which may enable the claim to stand separately even if Claim 9 falls.

VIII. Arguments

The claims present in this application stand rejected solely under the provisions of 35 U.S.C. §103(a). Accordingly, the only issue remaining in this Appeal is the obviousness of the claims of the application over Horita and Taguchi. Applicant respectfully submits that the claims would not have been obvious to one of ordinary skill in the art based upon a fair reading of the references so cited. Furthermore, applicant respectfully submits that the teachings of Horita and Taguchi cannot be combined as proposed by the Examiner to either teach or suggest each and every element of the claimed invention. Therefore, the claims are believed to be patentably distinguished over the cited references.

As stated herein, Claim 1 recites a circuit for generating a single asynchronous signal pulse at an output of an integrated circuit, including the following: (1) an

integrated circuit comprising a push-pull driving circuit having a first and second transistor including control terminals being independently controlled by different control pulses between a first and second supply potential, and a centre tap connected with an output terminal of the integrated circuit; and (2) a single resistor being externally coupled with the output terminal of the integrated circuit and being of a pull-up or pull-down type, wherein the type of the resistor determines, by application of a first control pulse on the control terminal of the second transistor and then a second control pulse on the control terminal of the first transistor, whether a single positive or a single negative control pulse being asynchronous to the applied control pulse and of the same duration is applied on the output terminal, wherein a waiting time is provided between the first control pulse and the second control pulse such that the two pulses do not overlap. Therefore, the application of an externally-coupled, pull-up or pull-down resistor determines whether the single pulse is a single negative or a single positive control pulse. This feature is advantageous because the negative or positive control pulse is provided at the output without special settings, such as circuit programming.

In contrast, Horita achieves the objective of providing an interconnection circuit for realizing fast signal transfers between semiconductor circuits. Horita, column 1, line 65, to column 2, line 9. In order to achieve this objective, the interconnection circuit of Horita provides for transferring a logic signal of a given level from one circuit to another circuit through a signal path therebetween. Horita, column 2, lines 2-9. The interconnection circuit includes a terminal resistor **R** to adjust the impedance of

the signal path **13** to a predetermined value. Horita, column 6, lines 43-47, and Figure 2 of the Drawings. Therefore, the function of the terminal resistor **R** of Horita is adjusting the voltage level at output terminal **OP1**. For example, when a low level **L** is applied on signal line **LG**, the voltage level at output terminal OP1 equals voltage **Vd** minus the threshold voltage of transistor **MP2** above the ground level, multiplied by the ratio of the resistance of the terminal resistor **R** to the sum of **R** and the ON-state resistor of transistor **MP2**. Horita, column 7, lines 28-33. Horita does not disclose a resistor coupled with the output of the integrated circuit and being of a pull-up or pull-down type, wherein the type of resistor determines whether a single positive or a single negative control pulse is applied on the output terminal. Rather, in the circuit disclosed by Horita, the generation of a negative or positive output from transistors **MP1** and **MP2** is determined by the output logic signal **LG** of CMOS circuit 11, not the terminal resistor **R**. Horita, column 7, lines 10-16 and 34-36. Therefore, applicant submits that Horita does not disclose each and every element of the claimed invention. Additionally, Horita offers no suggestion to modify the circuit disclosed therein to arrive at the presently claimed invention.

Furthermore, Claim 1 recites application of a first control pulse on the control terminal of the second transistor and then a second control pulse on the control terminal of the first transistor, wherein a waiting time is provided between the first control pulse and the second control pulse such that the two pulses do not overlap in time. Applicant respectfully submits that Horita does not disclose application of a first control pulse on the control terminal of the second transistor and then a second

control pulse on the control terminal of the first transistor, wherein a waiting time is provided between the first control pulse and the second control pulse such that the two pulses do not overlap in time.

Referring to Figure 2, for example, Horita teaches that CMOS circuit **11** can apply either a low level L or high level H to inverter **IN1**, **IN2**, and **IN3** for causing transistor **MP1** to be turned OFF and transistor **MP2** to be turned ON or vice versa, respectively. Horita, column 7, lines 5-9 and 18-22. Horita does not disclose applying a first control pulse on the control terminal of the second transistor and then a second control pulse on the control terminal of the first transistor, wherein a waiting time is provided between the first control pulse and the second control pulse such that the first and second pulses do not overlap in time. In fact, in Horita, there is only a single control signal **LG** which is applied nearly simultaneously, and thus overlapping in time, to the control terminals of the two transistors **MP1** and **MP2**. The difference in the time that the control signal reaches transistors **MP1** and **MP2** only results from the signal propagation delay caused by inverters **IN1**, **IN2**, and **IN3**. However, this delay caused by the signal propagation is not controllable in a way that the respective control terminals are being driven by a control signal being applied one after the other. Therefore, applicant submits that Horita does not disclose each and every element of the present invention because Horita does not disclose applying a first control pulse on the control terminal of the second transistor and then a second control pulse on the control terminal of the first transistor, wherein a waiting time is

provided between the first control pulse and the second control pulse such that the first and second pulses do not overlap in time.

Additionally, as noted above, Claim 1 recites an integrated circuit comprising control terminals being independently controlled by different control pulses between a first and second potential. Applicant respectfully submits that Horita does not teach an integrated circuit comprising control terminals being independently controlled by different control pulses between a first and second potential. Referring to FIG. 2 of Horita, for example, the inputs to inverters **IN1** and **IN2** are connected to a single signal, signal **LG**, output from CMOS circuit 11. The outputs of inverters **IN1** and **IN2** are connected to the inputs of transistors **MP1** and **MP2**. Horita, Figure 2 of the Drawings. Inverters **IN1** and **IN2** cannot be used to provide a control pulse to independently control the control terminals (i.e., the inputs) of transistors **MP1** and MP2 because the same signal **LG** must be input to inverters **IN1** and **IN2**. Because transistors **MP1** and **MP2** are connected to the output of inverters **IN1** and **IN2**, it therefore follows that transistors **MP1** and **MP2** are controlled solely by the same signal **LG** input into inverters **IN1** and **IN2**. Therefore, transistors **MP1** and **MP2** are not independently controllable. Thus, applicant respectfully submits that Horita does not disclose an integrated circuit comprising control terminals being independently controlled by different control pulses between a first and second potential. Therefore, applicant further urges that Horita does not disclose each and every element of the claimed invention. Additionally, Horita offers no suggestion to modify the circuit disclosed therein to arrive at the presently claimed invention.

Taguchi fails to overcome the significant shortcomings of Horita. Taguchi is directed to a system for transmitting a small-amplitude signal between a microprocessor **5** and a SDRAM **20** via a bus line **15**. Taguchi, column 1, lines 44-48. The system includes a push-pull-type output circuit **12** having a p-channel MOS transistor **13** functioning as a pull-up element and an n-channel MOS transistor **14** functioning as a push-down element. Taguchi, column 1, line 66, to column 2, line 2. As shown in Figure 3, transistors **13** and **14** are coupled in series between a line **26**, which supplies VCC power, and a line **27**, which supplies VSS power. Taguchi, column 2, lines 41-44. Microprocessor **5** includes an output terminal **6** connected to the coupling node of transistors **13** and **14** for connection to bus line **15**. Taguchi, Figure 3. Microprocessor **5** can transmit a low signal to SDRAM **20** by turning transistor **13** off and transistor **14** on. Taguchi, column 2, lines 22-27. Further, microprocessor **5** can transmit a high signal to SDRAM **20** by turning transistor **13** on and transistor **14** off. Taguchi, column 2, lines 27-29. Summarily, the system of Taguchi can transmit either a high or low signal on bus line **15** depending on the signal input into transistors **13** and **14**.

In contrast, the present invention, as claimed in amended Claim 1, applies only a single pulse on the output terminal in response to receiving both a positive and negative input pulse. The single input pulse is positive or negative depending on whether a single resistor, connected the output terminal, is of a pull-up or pull-down type. Thus, the output and input signals for the Taguchi system and the circuit of the presently claimed invention differ completely with regard to input and output.

Therefore, applicant respectfully submits that Taguchi does not teach or suggest each and every limitation of the presently claimed invention and, thus, cannot anticipate the presently claimed invention. Additionally, Taguchi offers no suggestion to modify the system disclosed therein to arrive at the presently claimed invention and, consequently, the combination proposed by the Examiner does not offer a reasonable chance of success in combining the cited references.

Moreover, the resistors of the presently claimed invention provide an entirely different function than the resistors of the Taguchi system. Regarding Taguchi, the disclosed system includes termination resistors **28**, **29**, **30**, and **31**. Taguchi, column 2, lines 45-50. Taguchi discloses that resistors **28**, **29**, **30**, and **31** are set approximately equal to 50 or 100 ohms. Taguchi, column 2, lines 46, 47, and 51-54. Resistors **28** and **29** and resistors **30** and **31** are connected in series across supply voltages **VCC** and **VSS**. Resistors **28**, **29**, **30**, and **31** appear to perform the function of stabilizing the signal differences between lines **15**, **26**, and **27**. In contrast, the single resistor recited in Claim 1 of the present application can be selected to be either a pull-up or pull-down type for determining whether a single positive or a single negative control pulse is applied on the output terminal. The single positive or single negative control pulse is applied on the output terminal in response to the application of a first control pulse on the control terminal of the second transistor and then a second control pulse on the control terminal of the first transistor. Thus, Taguchi does not teach each and every limitation of the presently claimed invention and, thus, cannot anticipate the presently claimed invention. Additionally, Taguchi offers no

suggestion to modify the system disclosed therein to arrive at the presently claimed invention.

As stated above, Claims 3–5 and 15 depend from Claim 1. Therefore, the comments presented above relating to Claim 1 apply equally to Claims 3–5 and 15. Furthermore, Claims 6 and 9 include limitations similar to those discussed above with regard to Claim 1. Claims 7, 8, and 16 depend from Claim 6, and Claims 10 and 11 and 17 depend from Claim 9. Thus, the comments presented above relating to Claim 1 apply equally to Claims 7, 8, 10, 11, 16, and 17.

Applicant respectfully submits that the teachings of Horita and Taguchi cannot be combined to either teach or suggest each and every element of the present invention. Additionally, neither Horita nor Taguchi offer a suggestion to modify the circuit disclosed therein to arrive at the presently claimed invention. Therefore, Claims 1, 3–11, and 15–17 are believed to be patentably distinguished over the cited references. Applicant respectfully submits that the rejections are based upon improper combinations and modifications of the references. Accordingly, applicant respectfully requests the reversal of the rejections of Claims 1, 3–11, and 15–17 under 35 U.S.C. §103(a).

Serial No.: 10/052,652

The Commissioner is hereby authorized to charge any fees associated with the filing of this correspondence to Deposit Account No. **50-0426.**

Respectfully submitted,

JENKINS, WILSON & TAYLOR, P.A.

Date: 3-1-04 By: Richard E. Jenkins

Richard E. Jenkins
Registration No. 28,428
Customer No: 25297

1403/36 REJ/BJO/alb

Appendix

1. A circuit for generating a single asynchronous signal pulse at an output of an integrated circuit, the circuit comprising:

   (a) an integrated circuit comprising a push-pull driving circuit having a first and second transistor including control terminals being independently controlled by different control pulses between a first and second supply potential, and a centre tap connected with an output terminal of the integrated circuit; and

   (b) a single resistor being externally coupled with the output terminal of the integrated circuit and being of a pull-up or pull-down type, wherein the type of the resistor determines, by application of a first control pulse on the control terminal of the second transistor and then a second control pulse on the control terminal of the first transistor, whether a single positive or a single negative control pulse being asynchronous to the applied control pulse and of the same duration is applied on the output terminal,

   wherein a waiting time is provided between the first control pulse and the second control pulse such that the two pulses do not overlap.

2. (Canceled)

3. The circuit as claimed in claim 1, wherein one of the two control pulses is generated from the other of the two control pulses by an inverter delay device.

4. The circuit as claimed in claim 1, wherein the first transistor is a P-channel MOS transistor and the second transistor is an N-channel MOS transistor, the control connection of the first transistor being inverted.

5. The circuit as claimed in claim 4, wherein the first transistor and the second transistor form a CMOS inverter with independent control gate connections.

6. A circuit for generating a negative signal pulse in response to receiving a sequence of a positive and negative control pulse, the circuit comprising:

(a) a first transistor including a control terminal and a load path connected between an output terminal and a first supply potential for receiving a negative control pulse at the control terminal;

(b) a second transistor including a control terminal and a load path connected between the output terminal and a second supply potential having a potential less than the first supply potential for receiving a positive control pulse at the control terminal in a sequence with the control terminal of the first transistor receiving the negative control pulse; and

(c) a pull-up resistor connected between the first supply potential and the output terminal for generating a negative signal pulse at the output terminal in response to the control terminals receiving the sequence of negative and positive control pulses.

7. A circuit according to claim 6 wherein a waiting time is provided between the sequence of negative and positive control pulses such that the control pulses do not overlap.

8. A circuit according to claim 6 further including an inverter delay device for generating one of the first and second control pulses from the other of the two control pulses.

9. A circuit for generating a positive signal pulse in response to receiving a sequence of a positive and negative control pulse, the circuit comprising:

(a) a first transistor including a control terminal and a load path connected between an output terminal and a first supply potential for receiving a negative control pulse at the control terminal;

(b) a second transistor including a control terminal and a load path connected between the output terminal and a second supply potential having a potential less than the first supply potential for receiving a positive control pulse at the control terminal in a sequence with the control terminal of the first transistor receiving the negative control pulse; and

(c) a pull-down resistor connected between the second supply potential and the output terminal for generating a positive signal pulse at the output terminal in response to the control terminals receiving the sequence of negative and positive control pulses.

10. A circuit according to claim 9 wherein a waiting time is provided between the sequence of negative and positive control pulses such that the control pulses do not overlap.

11. A circuit according to claim 9 further including an inverter delay device for generating one of the first and second control pulses from the other of the two control pulses.

12-14. (Not Entered)

15. A circuit according to claim 1 wherein the first and second transistors include a source and drain, the drain of the first transistor being connected to the drain of the second transistor, the source of the first transistor being connected to the first supply potential, and the source of the second transistor being connected to the second supply potential.

16. A circuit according to claim 6 wherein the first and second transistors include a source and drain, the drain of the first and second transistor being connected to the output terminal, the source of the first transistor being connected to the first supply potential, and the source of the second transistor being connected to the second supply potential.

17. A circuit according to claim 9 wherein the first and second transistors include a source and drain, the drain of the first and second transistor being connected to the output terminal, the source of the first transistor being connected to the first supply potential, and the source of the second transistor being connected to the second supply potential.